— IGFET

MOSFET

metal oxide semiconductor field effect transistor

construction. working → electric field

we know

$$V = -\int \vec{E} \cdot d\vec{l}$$

due to electric field → width of channel (Path of I)

$R_{ch} = \frac{l}{\sigma A}$, A↑ , $R_{ch}\downarrow$ I↑

I is controlled by E- field or voltage.

- it is also known as voltage controlled current source.

MOSFET have 3 terminal

- Source
- Drain
- gate → control terminal → it generate E-field to control I flow b/w source & ~~control~~ drain

$\downarrow$

oxide (SiO_2)

$I_g = 0$

— IGFET

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  ↓

  oxide (SiO_2)

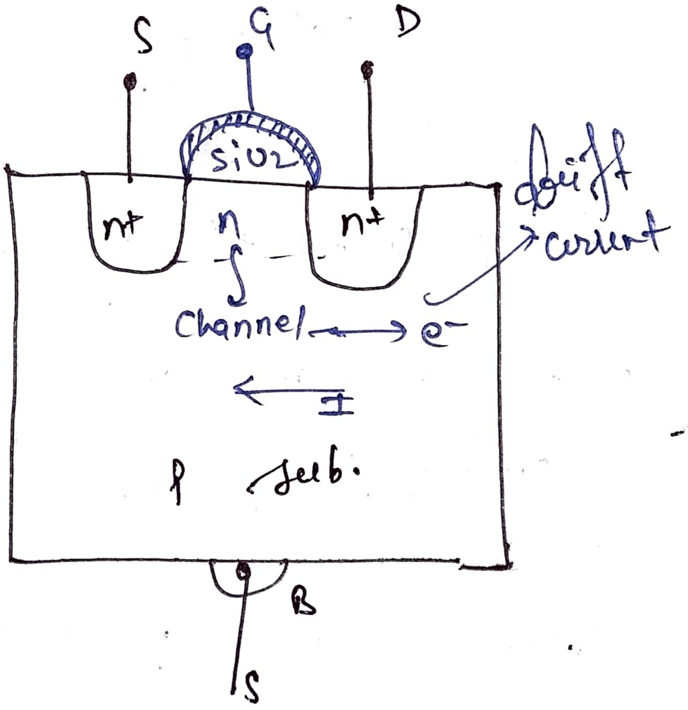
  $I_g = 0$

- Input impedence of MOSFET is around infinite
- it is smaller in size than BJT
- But A_v (MOS) < A_v (BJT) A_v = voltage gain.

MOSFET type
- Depletion
  - n-channel
  - p-channel
- enhancement

a) Depletion type ✓

- n-channel
- $W_{oxide} \simeq 1000 \sim 2000$ A°
- it is symmetrical device Drain & Source can be interchanged.



- Z_{in} = high
- b/w gate & body of it act as capacitor.
- MOSFET is unipolar device
- Gen. we use common source

Case I :-

$V_{GS} = 0, \quad V_{DS} = 0$

$I_{DS} = 0, \quad I_D = 0$

drain to source current

Case II :-

$V_{GS} = 0, \quad V_{DS} > 0$

$I_{DS} > 0$ (Drain to source.)

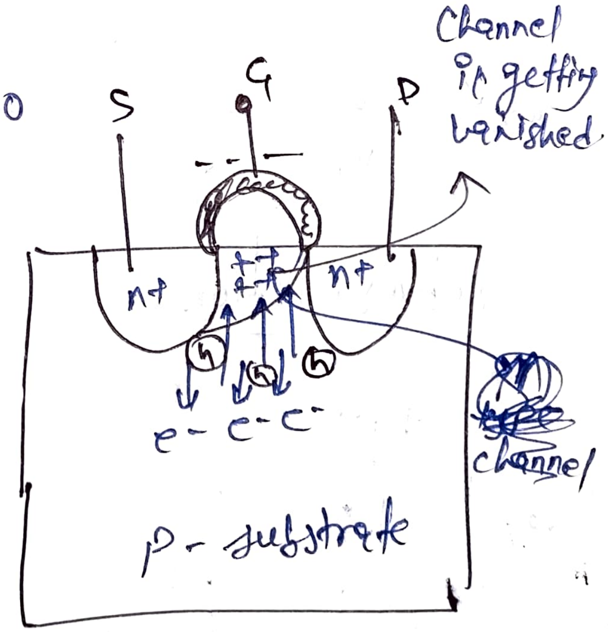
if $V_{DS} < 0$

then current flow source to Drain.

- MOSFET is bidirectional device.

Case III :-

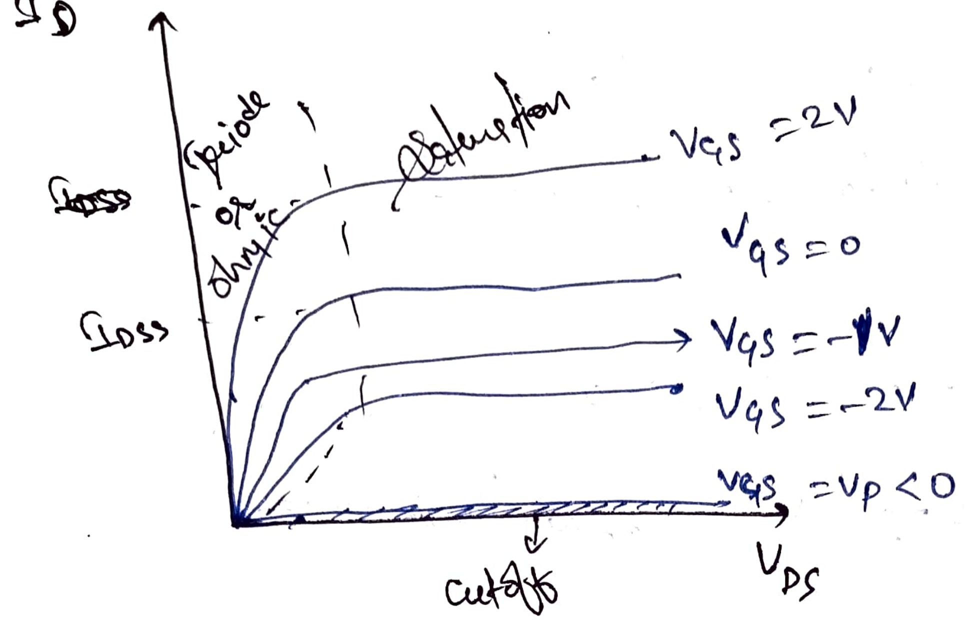
$V_{GS} < 0, \quad V_{DS} > 0$



As drain voltage is higher than source so channel vanish first from drain side.

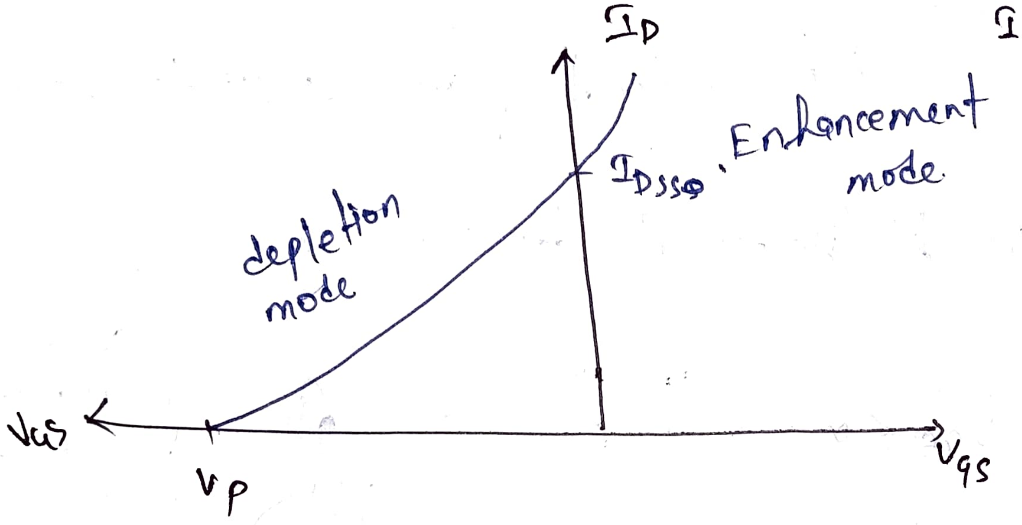
when there is no channel ~~is~~ this cond^n is known as pinch off.

① output ~~characteristist~~ characteristics

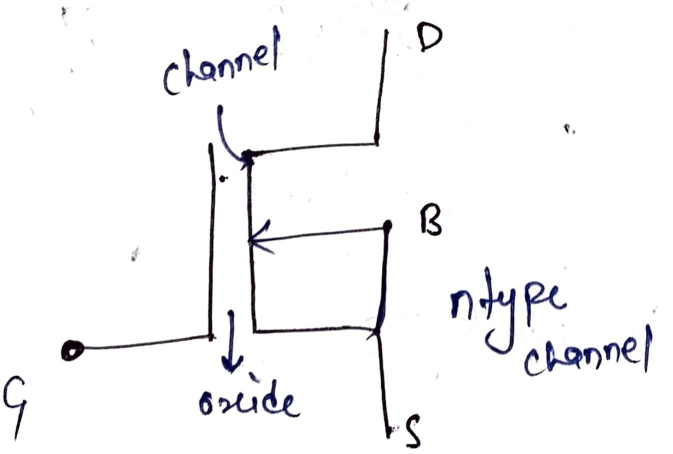


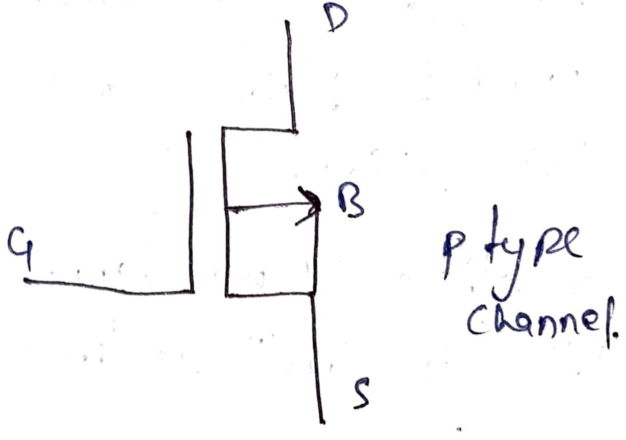
if $V_{GS} < 0$
channel width reduces
$R_{ch} = \rho \frac{l}{A} \uparrow$
$I_D \downarrow$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$



Representation





if body is shorted to source
then it acts as 3 terminal voltage

← Region of operation:→

Pinch of voltage: ⇒ Gate source voltage at which no channel exist ($I_D = 0$)

⇓

threshold voltage:

- cut off region:

$$V_{GS} < V_T \quad , I_D = 0$$

- Triode or ohmic region:

$$V_{GS} > V_T \quad , V_{DS} \leq V_{GS} + |V_T|$$

$$I_D = 2K\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$K = \mu_n C_{ox} \frac{W}{2L}$$

$$K_a = K_n\left(\frac{w}{2L}\right)$$

$$K_n = \mu_n C_{ox}$$

μ_n = mobility of e^-

C_{ox} = oxide capacitance (f/cm²)

W = channel width

L = channel length

Saturation region: →

$$V_{GS} \geq V_T \quad , V_{DS} \geq V_{GS} + V_T$$

$$I_D = K(V_{GS} + |V_T|)^2$$

when $V_{GS} = 0$, $I_D = I_{DSS}$

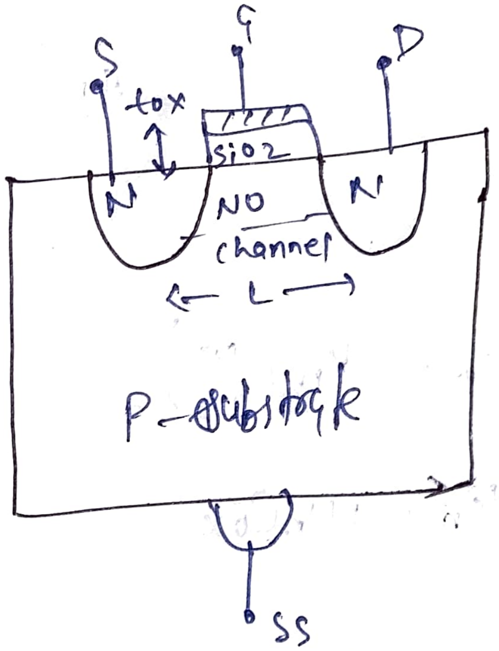
$$I_{DSS} = K|V_T|^2$$

$$K = \frac{I_{DSS}}{|V_T|^2} ,$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_T}\right)^2 .$$

← Enhancement type MOSFET → tox → oxide width

- channel is not formed by dopping
- fabrication cost is reduced.



substrate or body

Case I

$V_{GS} = 0, V_{DS} = 0$

$I_D = 0$

Case II $V_{GS} = 0, V_{DS} > 0$

no channel present hence

$I_D = 0$

Case 3:

when V_{GS} is varies → Accumulation mode
→ depletion mode
→ inversion mode.

Accumulation mode

. when $V_{GS} < 0$

- P-type → majority: holes
- Fh → dir" of E-field
- holes accumulate under gate
- no channel formation $I_D = 0$

depletion mode

' when $V_{GS} > 0$

$0 < V_{GS} < V_T$
⇓
depletion region

- hole is llel to E-field
- hole move away from gate terminal.
- channel region is depleted of charge chr carriers.
- no channel formation, $I_D = 0$.

Inversion mode

V_{GS} = high > 0

~~$0 < V_{GS} < V_T$~~

- holes move away from channel
- minority carriers electron's moves toward gate terminal.
- In channel region when $\boxed{n > p}$ → n-type material
channel is formed.

threshold voltage: min. value of V_{gs} at which inversi

take place.

$\frac{W}{L}$ = aspect ratio of Mosfet

$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ F/cm² (cap. per unit area).

Region of operations:-

1). $V_{gs} < V_T$

- no channel is formed

$I_D = 0$

$V_T > 0$ (n- channel MOS)

I_D does not depend on V_{DS}

2) linear or Triode region:-

$V_{gs} > V_T$

- channel is formed

then $V_{DS} < V_{gs} - V_T$

$$I_D = 2K\left[(V_{gs} - V_T) V_{DS} - \frac{V_{DS}^2}{2}\right]$$

Saturation region:-

$V_{GS} > V_T$

$V_{DS} > (V_{GS} - V_T)$

Channel starts to vanish. near drain

$$I_D = K\left[(V_{GS} - V_T)\right]^2$$

$$K = \mu_n C_{ox} \frac{W}{2T} \frac{(A/V^2)}{unit}$$

as $V_{DS} \uparrow$, $L \downarrow$, channel length modulation

<u>ideal</u>

$$I_D = K(V_{GS} - V_T)^2$$

<u>Practically</u>, due to channel length modulation

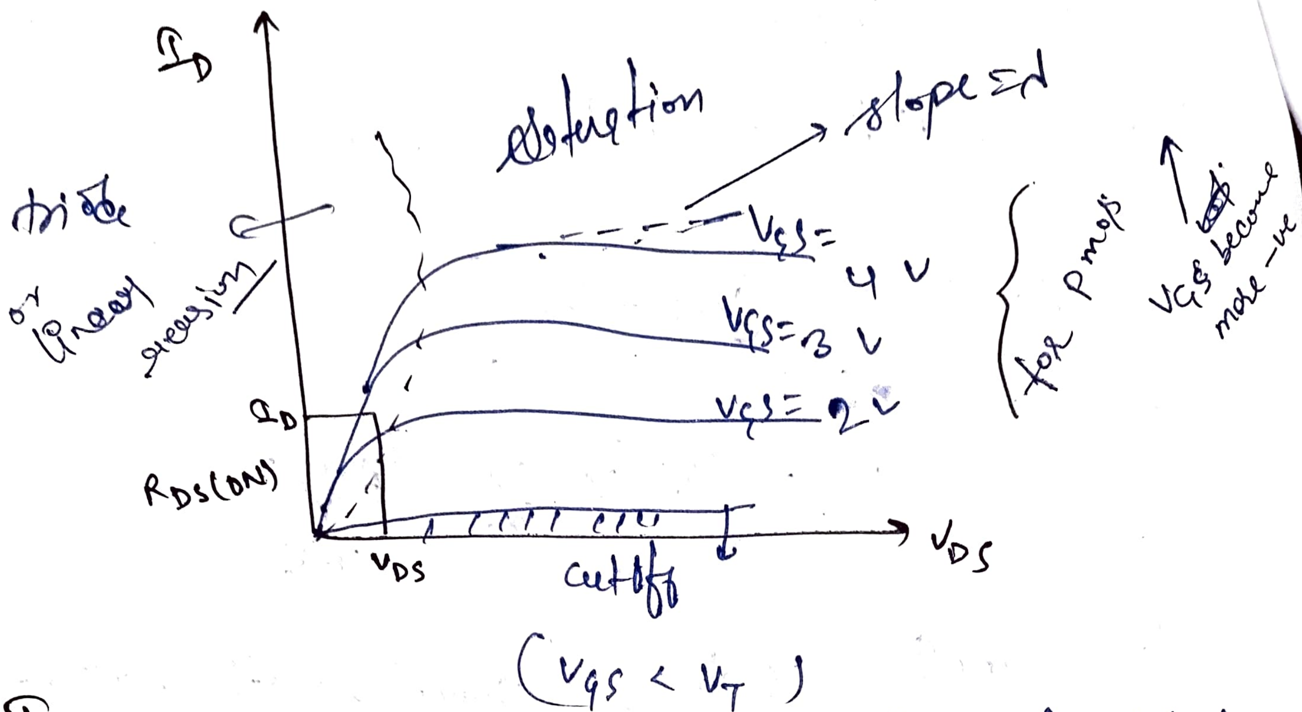
$$I_D = f(V_{DS})$$

$$I_D = K(V_{GS} - V_T)^2\left[1 + \lambda V_{DS}\right]$$

λ = channel length modulation.

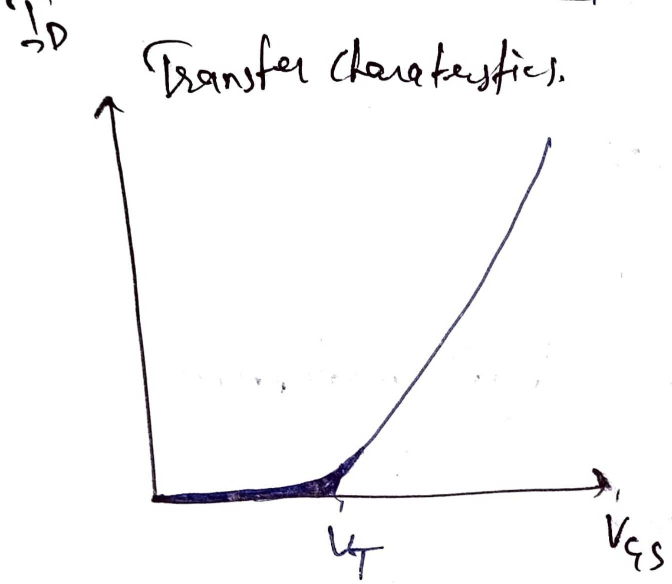
Characterstics of n-mos

O/P charac



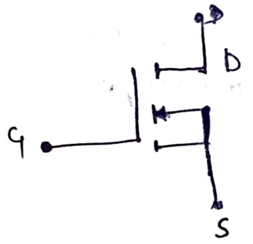
$I_D \propto (1+\lambda V_{DS})$

Transfer charateristics.

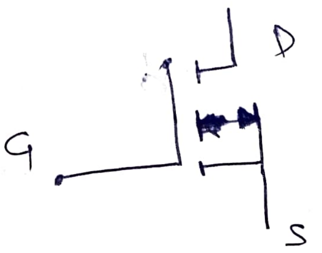


$I_D = K\cdot(V_{GS}-V_T)^2$

Enhancement type MOSFET symbols:-

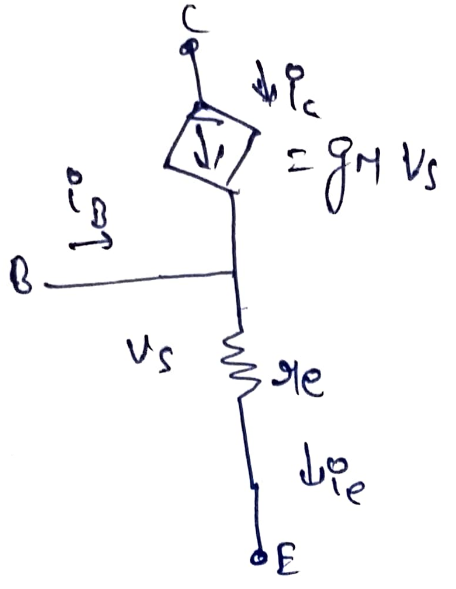


n- channel



p-channel

T model



$$g_m = \frac{I_C}{V_T}$$

$$r_e = \frac{V_T}{I_E} = \frac{\alpha}{g_m}$$

$$\alpha = g_m r_e$$

*

$R_{in} = r_\pi$

$A_{vo} = -g_m R_C$

$R_o = R_C$

$A_v = A_{vo} \dfrac{R_L}{R_L + R_o}$ or $-g_m (R_C \| R_L)$

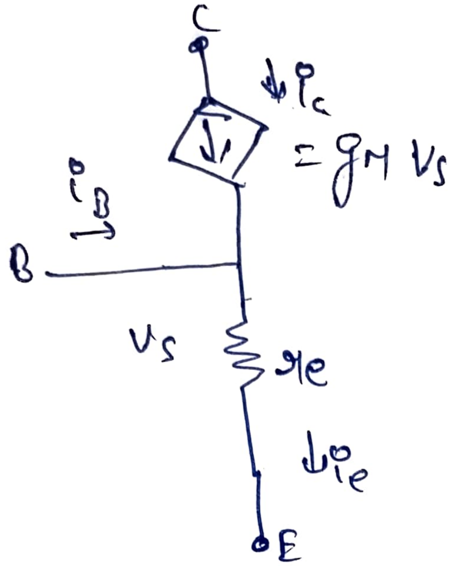
overall voltage gain

$$G_v = \frac{R_{in}}{R_{in} + R_{sig}} A_v$$

$$V_{sig} = \frac{R_{in} + R_{sig}}{R_{in}} \cdot V_\pi$$

$$V_o = G_v V_{sig}$$

T model



$$g_m = \frac{I_c}{V_T}$$

$$r_e = \frac{V_T}{I_E} = \frac{\alpha}{g_m}$$

$$\alpha = g_m r_e$$

*

$R_{in} = r_\pi$

$A_{vo} = -g_m R_c$

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$A_v = A_{v_o} \dfrac{R_L}{R_L + R_o}$ or $-g_m (R_c \| R_L)$

overall voltage gain

$$G_v = \frac{R_{in}}{R_{in} + R_{sig}} A_v$$

$$V_{sig} = \frac{R_{in} + R_{sig}}{R_{in}} \cdot V_\pi$$

$$V_o = G_v V_{sig}$$

MOSFET AS SWITCH

SFET:- is a voltage control device, it can be used with micro controller also.

More power efficient as compare to BJT

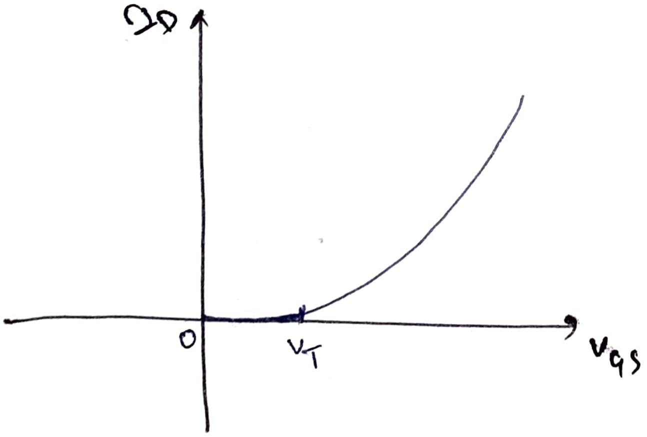
There are two type of losses when MOSFET OR BJT are used as switches:-

- conduction loss
- switching loss

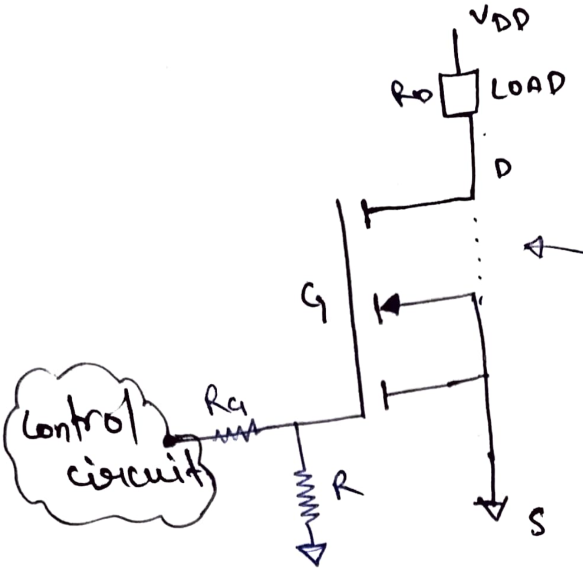
- MOSFET are more thermally stable as compare to BJT because MOSFET has +ve temp. co-efficient.

$$\text{As } T\uparrow \Rightarrow R_{DS(ON)}\uparrow \Rightarrow I_D\downarrow$$

- Enhancement type MOSFET are used for switches



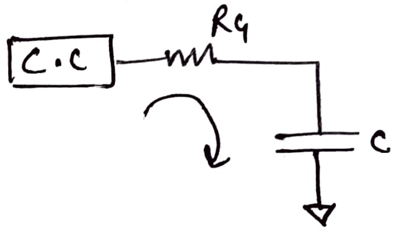
n type MOSFET



- when $V_{GS} < V_T$
  no current flow (off)

- when $V_{GS} > V_T$
  (Closed ckt) (ON)

Gate to source ckt
before R

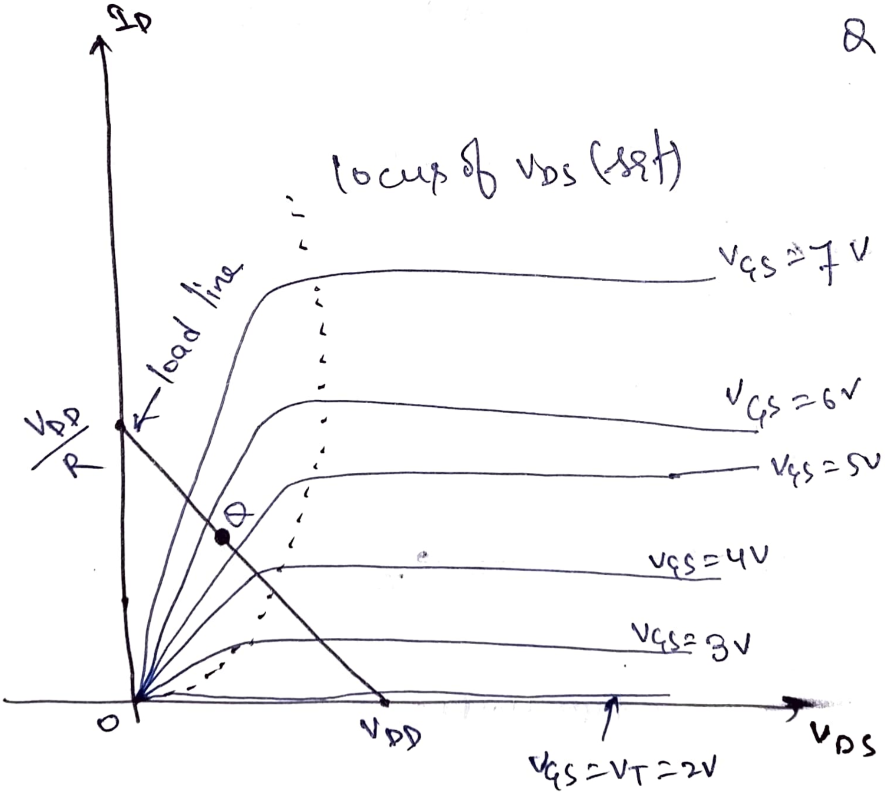


let load R_D, $V_{DS} = 0$

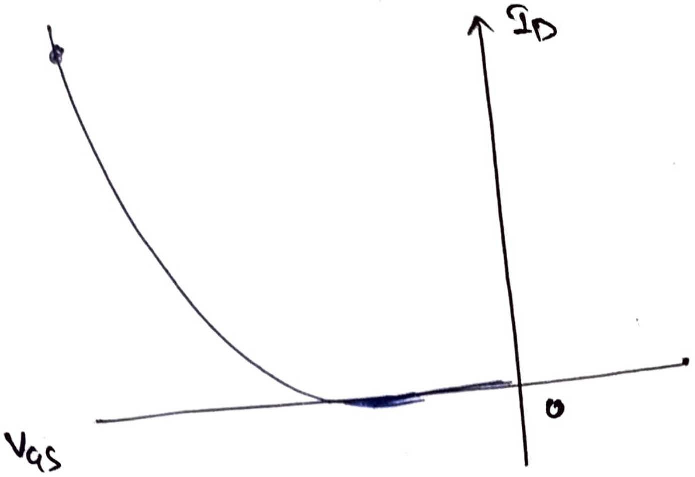
$$I_D = \frac{V_{DD}}{R_D}$$

if $I_D = 0$, ⇒ $V_{DS} = V_{DD}$

Q → operating point

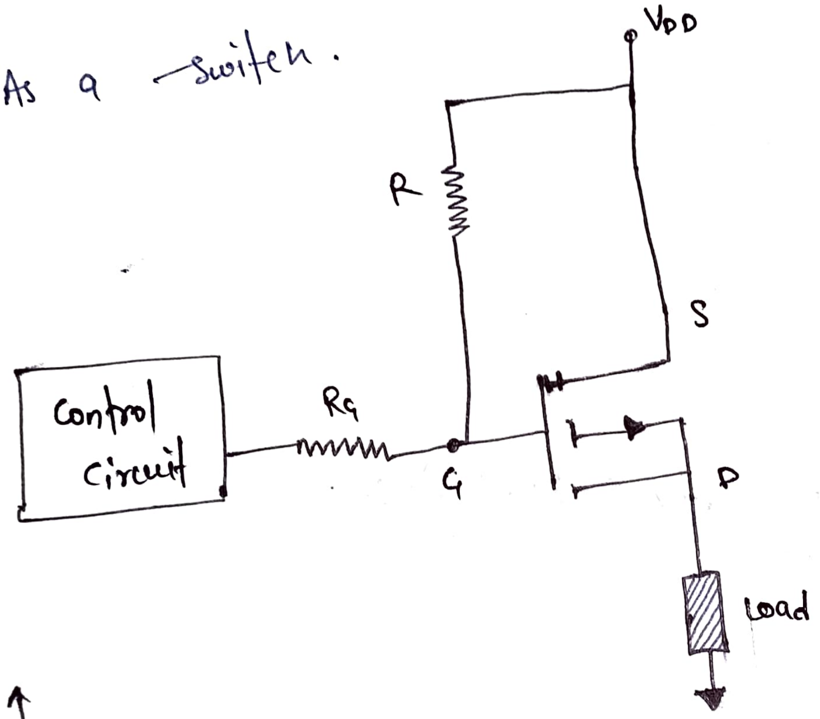


P channel

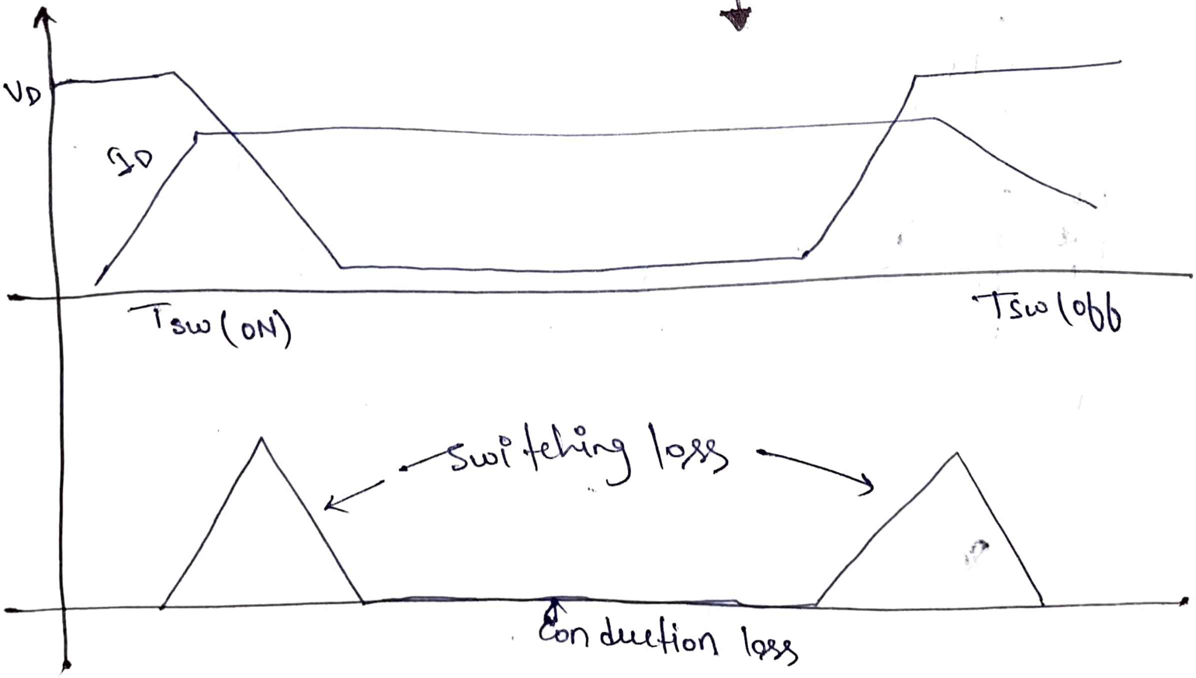


P-type MOSFET

As a switch.



$V_{GS} = 0$



—: MOSFET Biasing Depletion Type MOSFET :—

for n channel,

to be in saturation region (active mode)

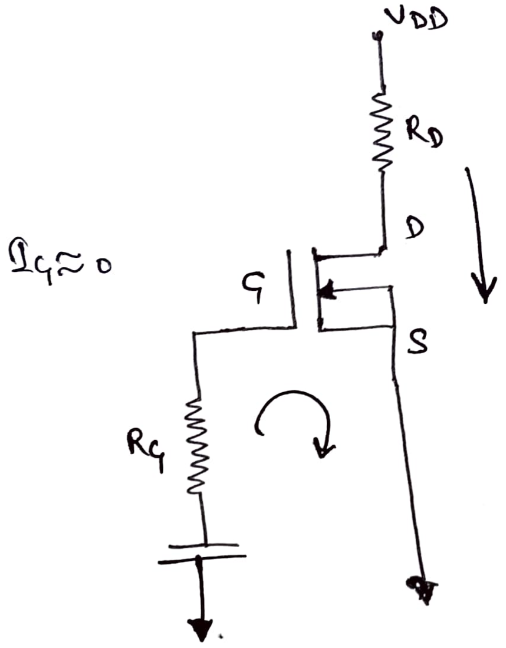
$V_{DS} \geq V_{GS} - V_P$

$|V_{GS}| < |V_P|$ & $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

there are three type of biasing can be done in MOSFET :—

- fixed biasing
- self biasing
- Voltage divider biasing.

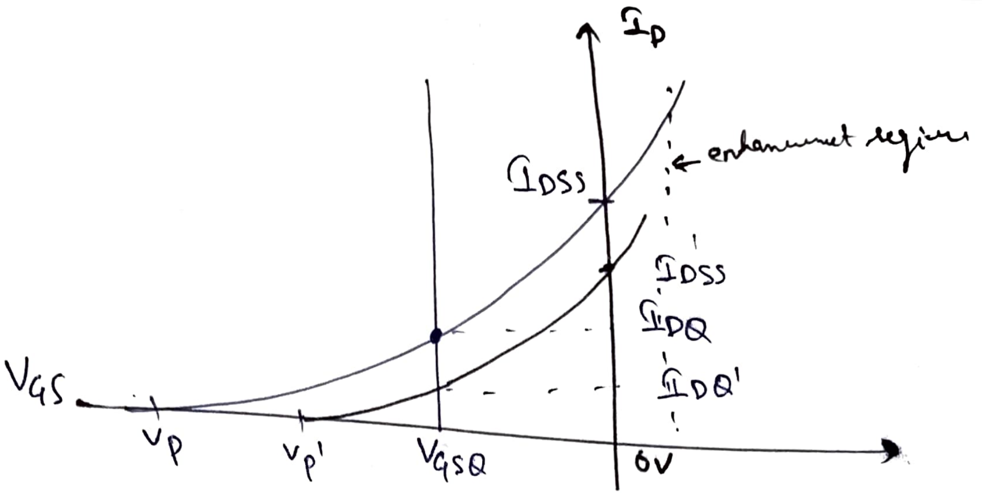
Depletion type MOSFET (fixed biasing) :—



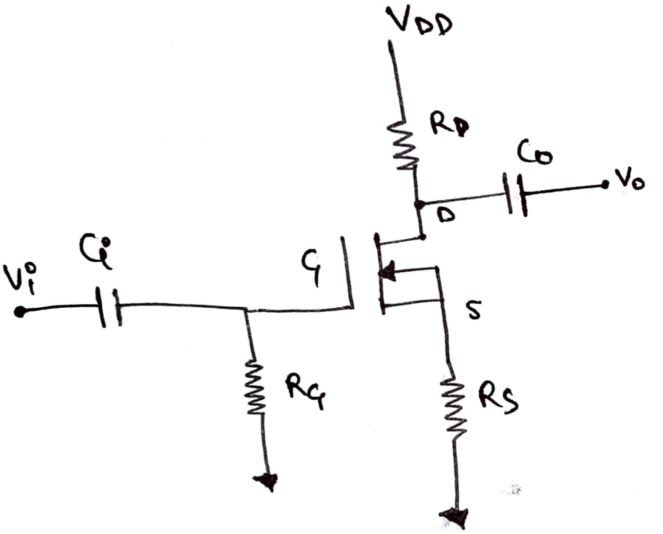
$V_{GS} = -V_{GG}$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \quad -(1)$$

$$V_{DS} = V_{DD} - I_D R_D \quad -(2)$$



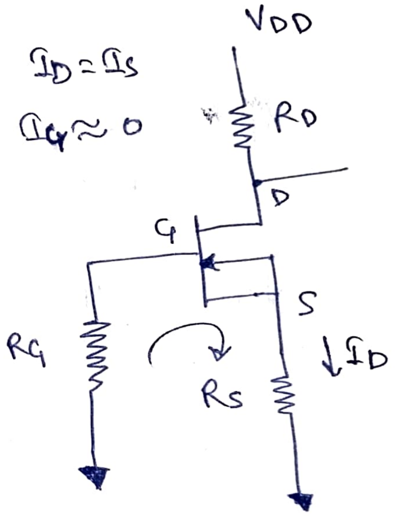
Depletion type MOSFET (Self Biasing) :—



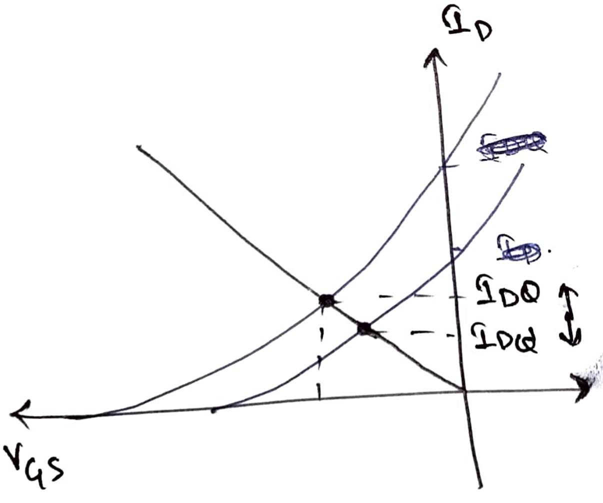
DS equⁿ ⇒

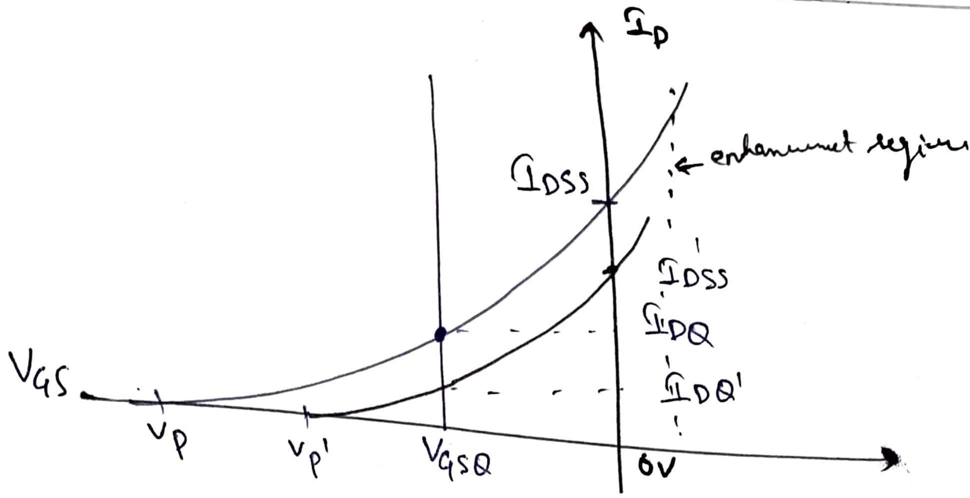
$I_D = I_S$

$I_G \approx 0$

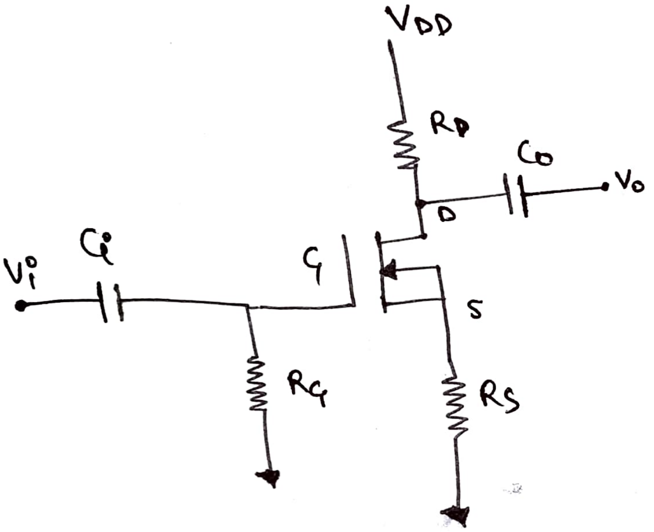


- $V_{GS} = -I_D R_S$
- $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$
- $V_{DS} = V_{DD} - I_D(R_D + R_S)$





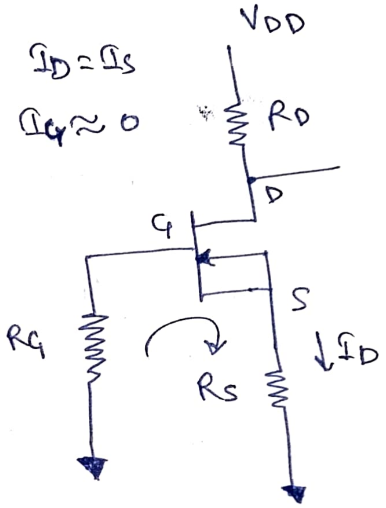
Depletion type MOSFET (Self Biasing) :—



DC equ ⇒

$I_D = I_S$

$I_G \approx 0$



- $V_{GS} = -I_D R_S$
- $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$
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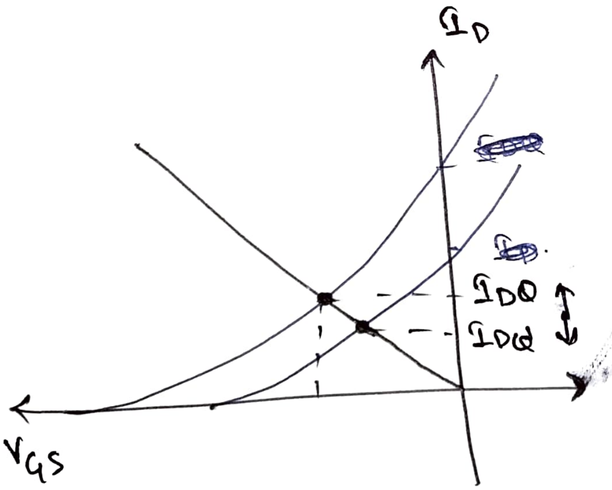
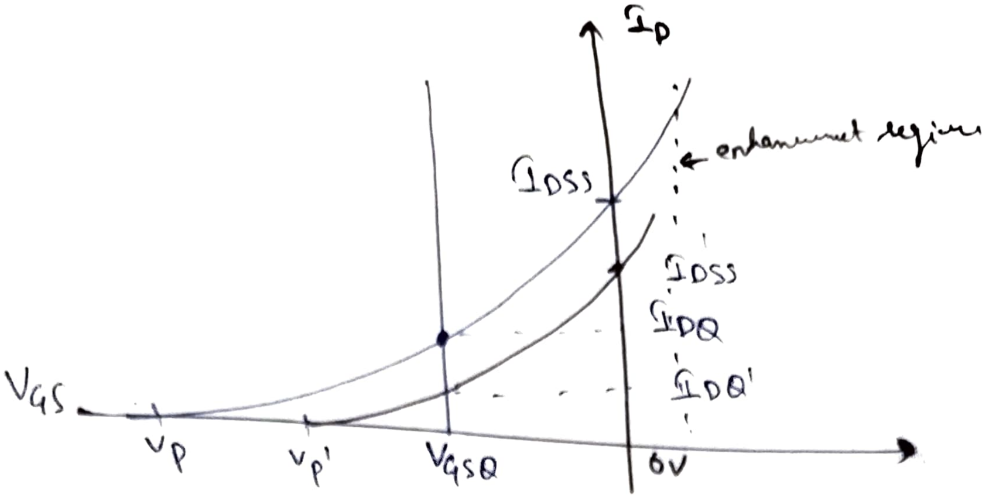
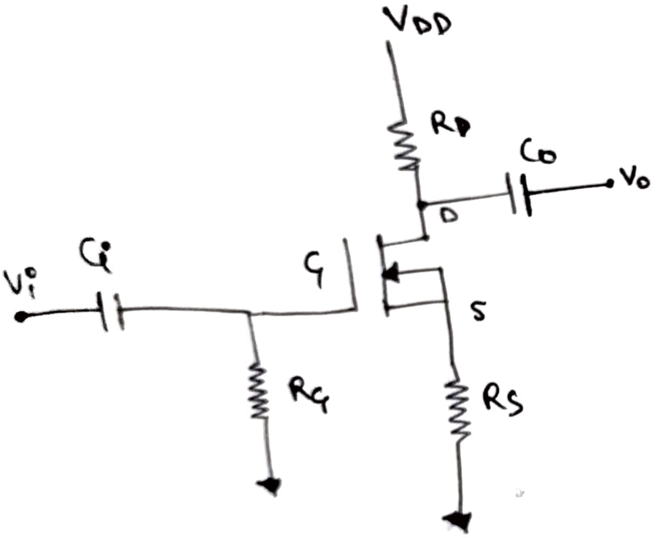




Depletion type MOSFET (Self Biasing):—



DC equ ⇒

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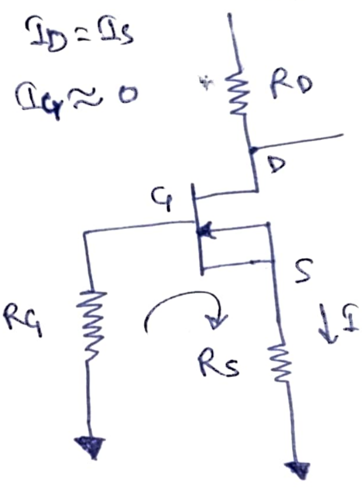
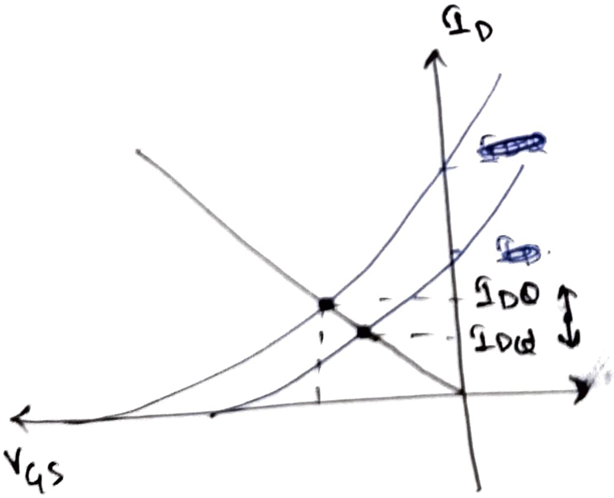
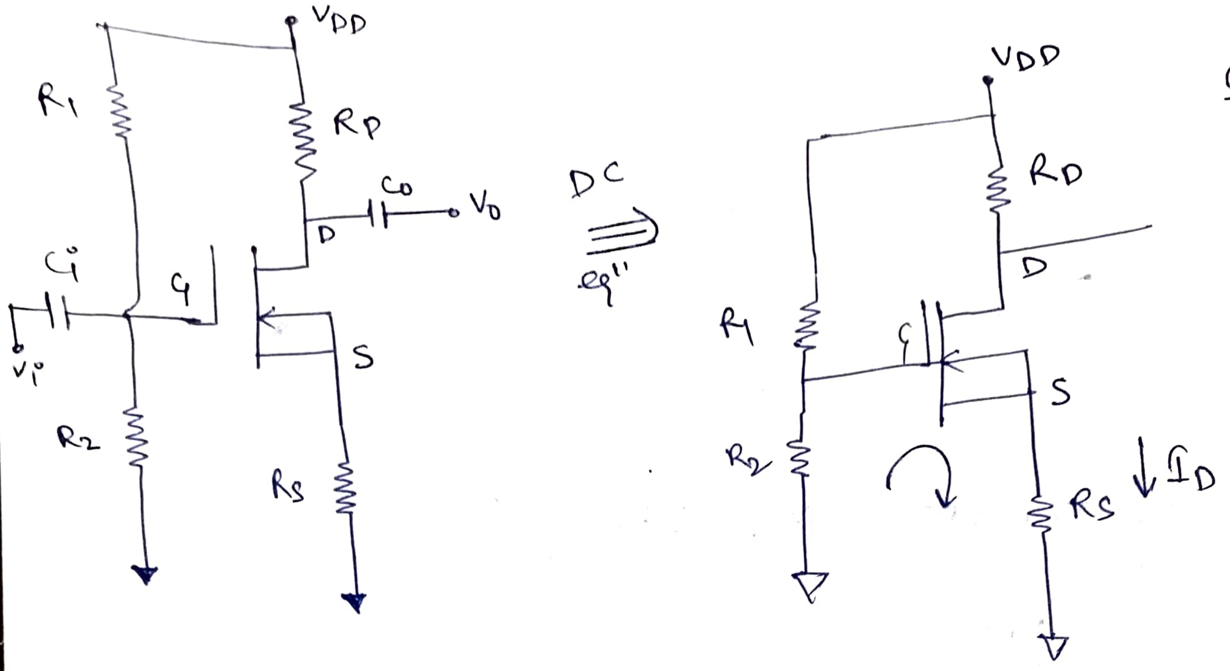


- $V_{GS} = -I_D R_S$
- $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$
- $V_{DS} = V_{DD} - I_D(R_D + R_S)$

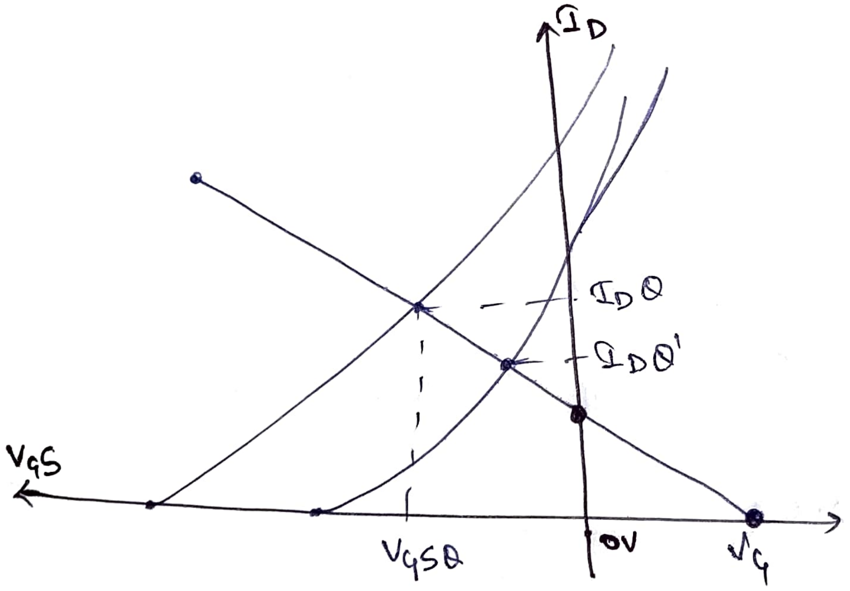


Depletion type MOSFET (voltage divider Biasing



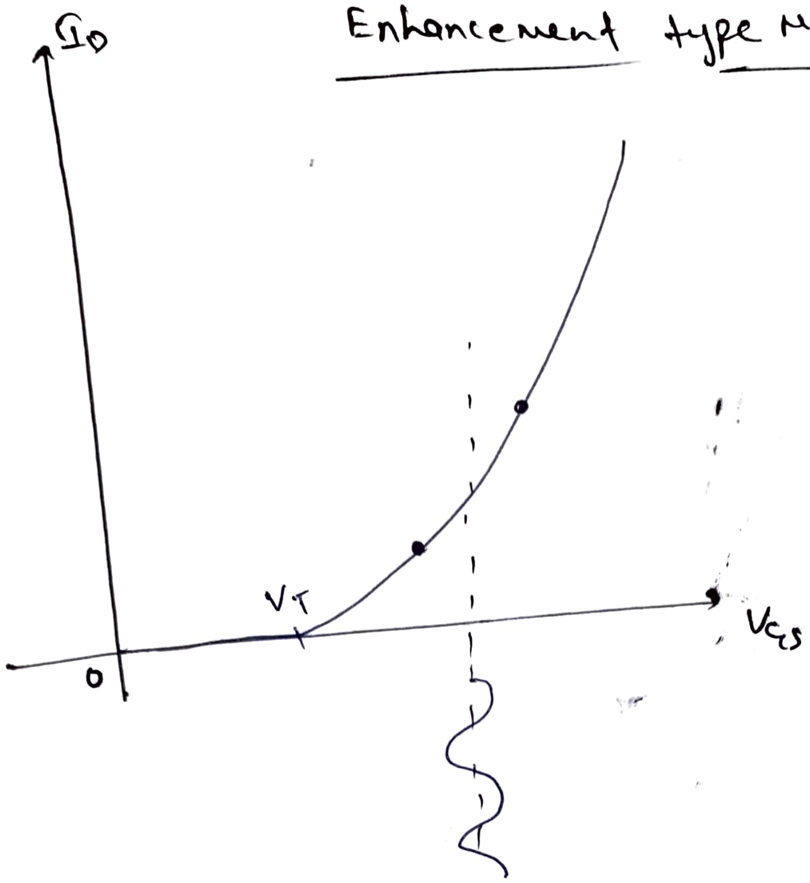
$I_G \simeq 0$

- $V_G = \frac{R_2}{R_1 + R_2} \cdot V_{DD}$
- $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$
- $V_{GS} = V_G - I_D R_D$
- $V_{DS} = V_{DD} - I_D(R_D + R_S)$

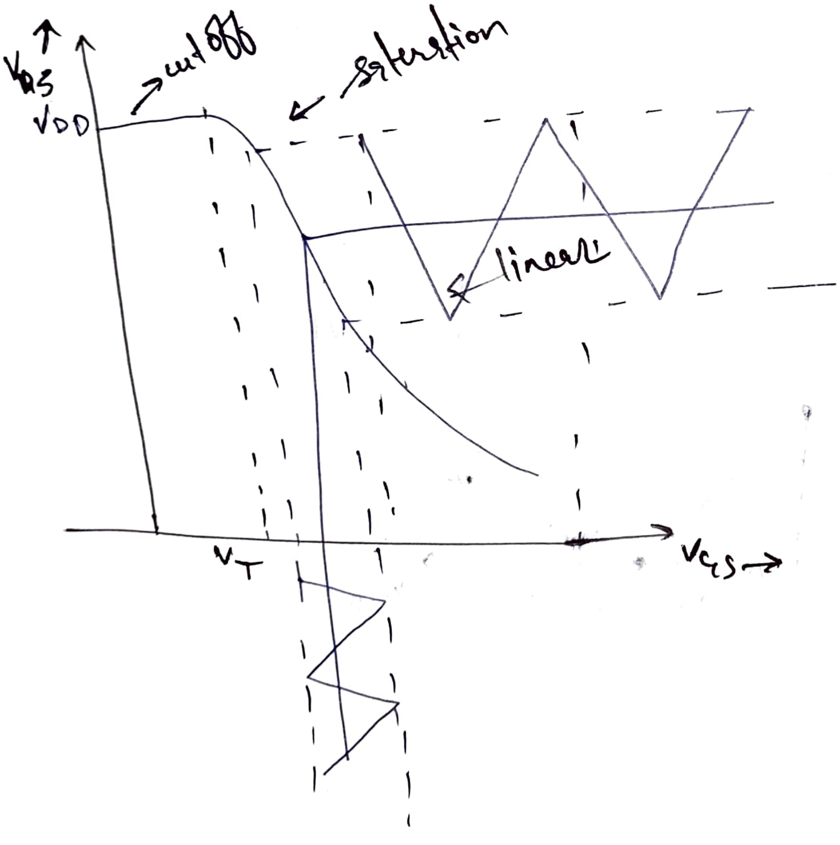


$I_D = \frac{V_G}{R_S}$

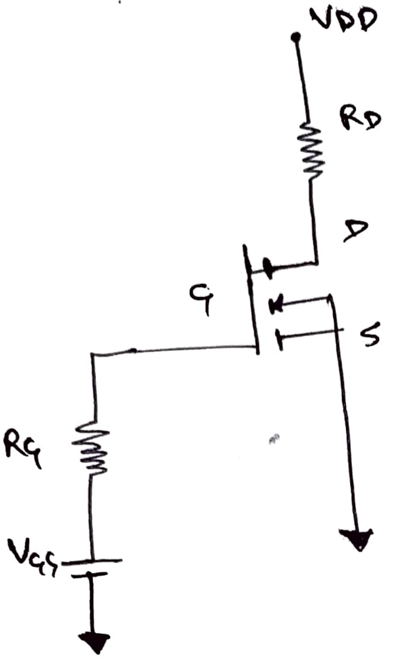
Enhancement type MOSFET



voltage transfer characteristics of the MOSFET:—



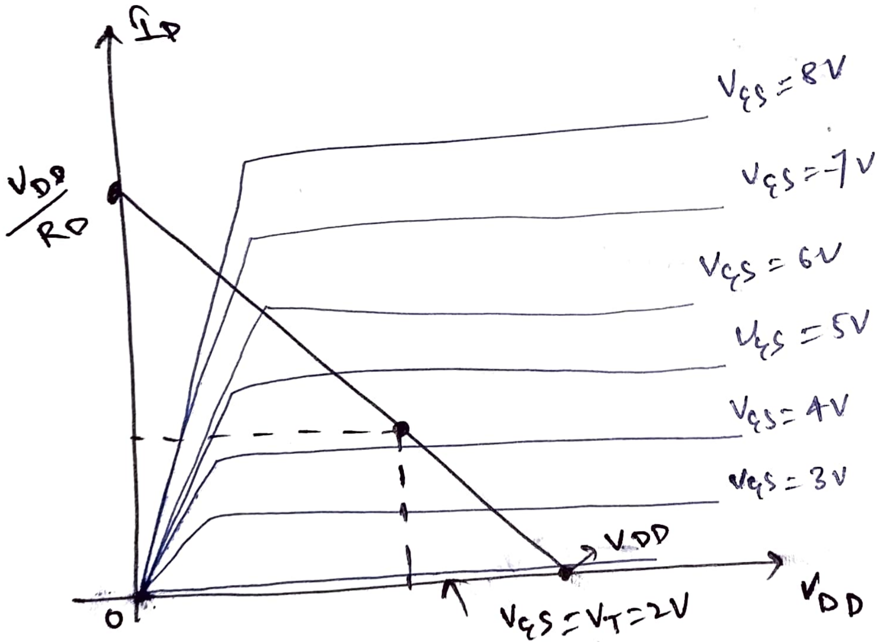
–: MOSFET Biasing:–



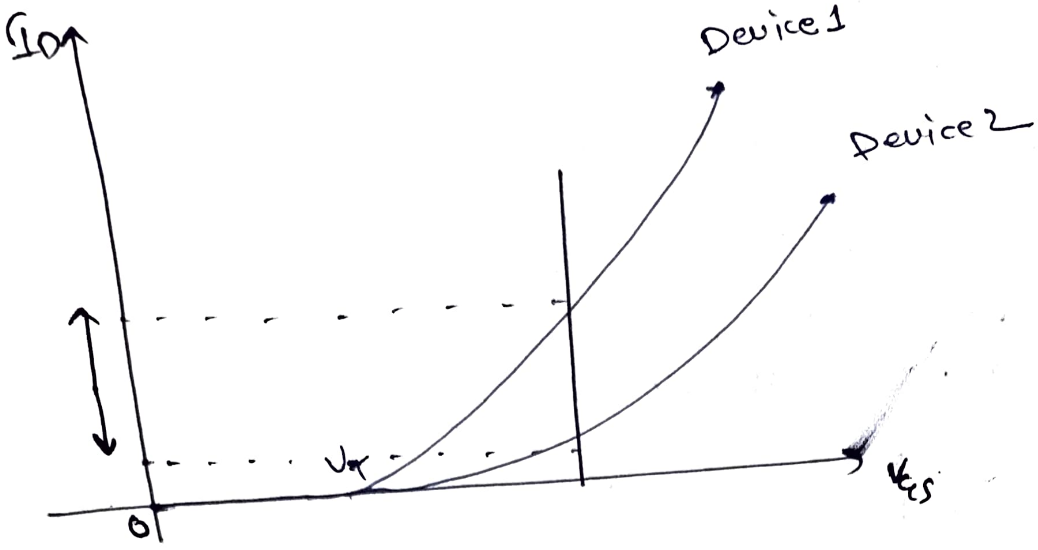
$$I_D = K(V_{GS} - V_T)^2$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\left[\frac{W}{L}\right](V_{GS} - V_T)^2$$

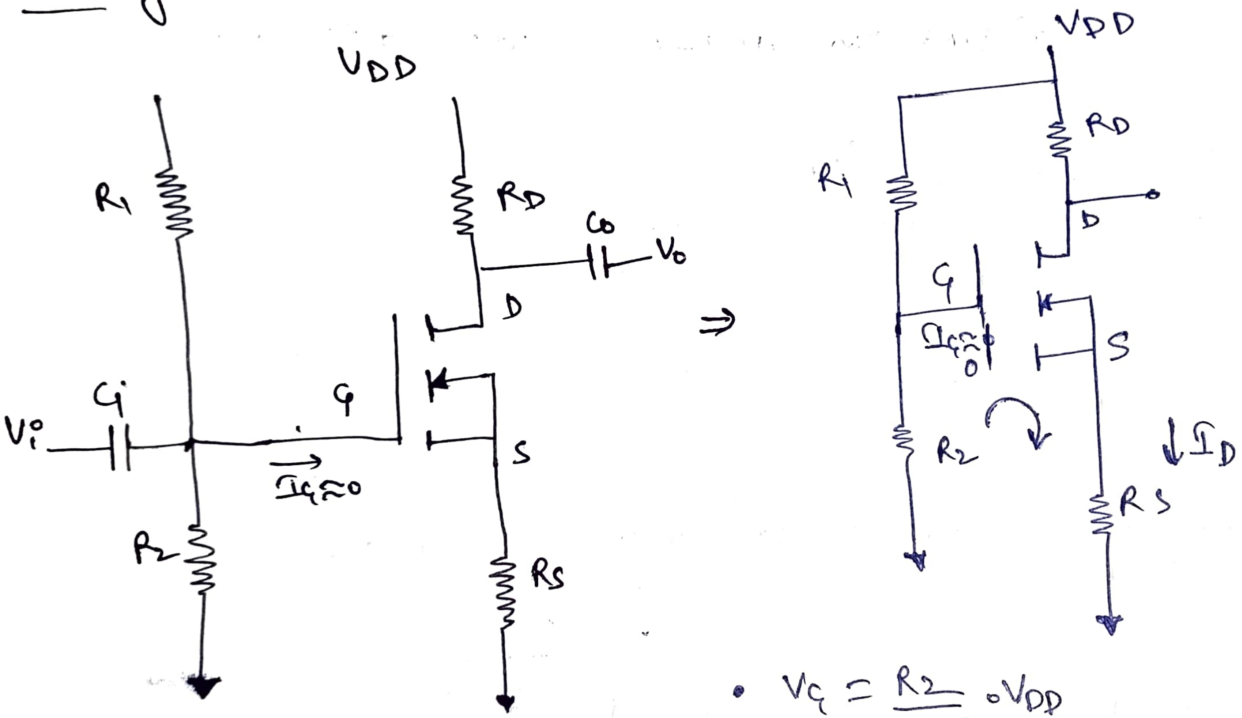
Enhancement type MOSFET (Drain characteristics):–



Transfer characteristics of Enhancement type MOSFET



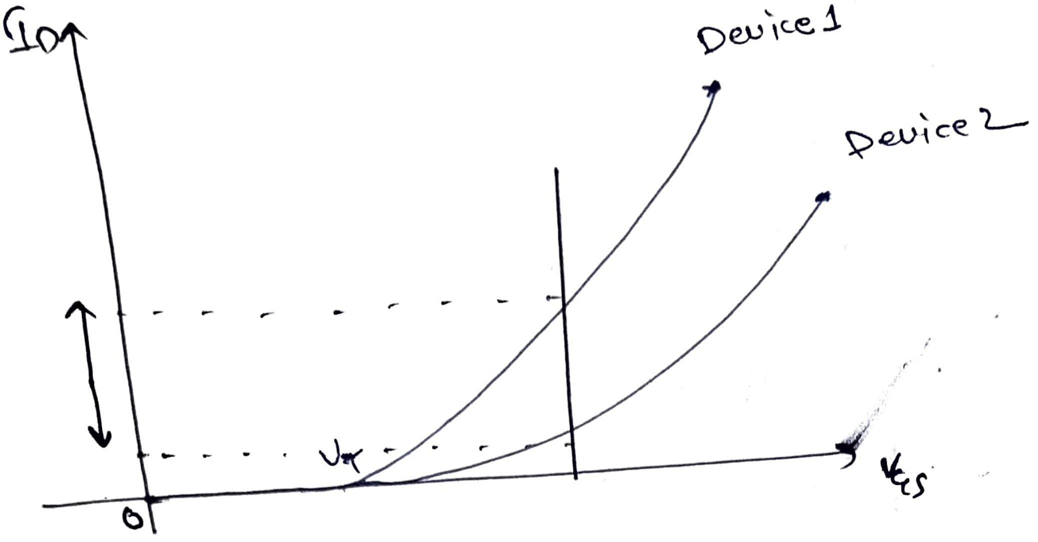
Voltage Divider Biasing:—



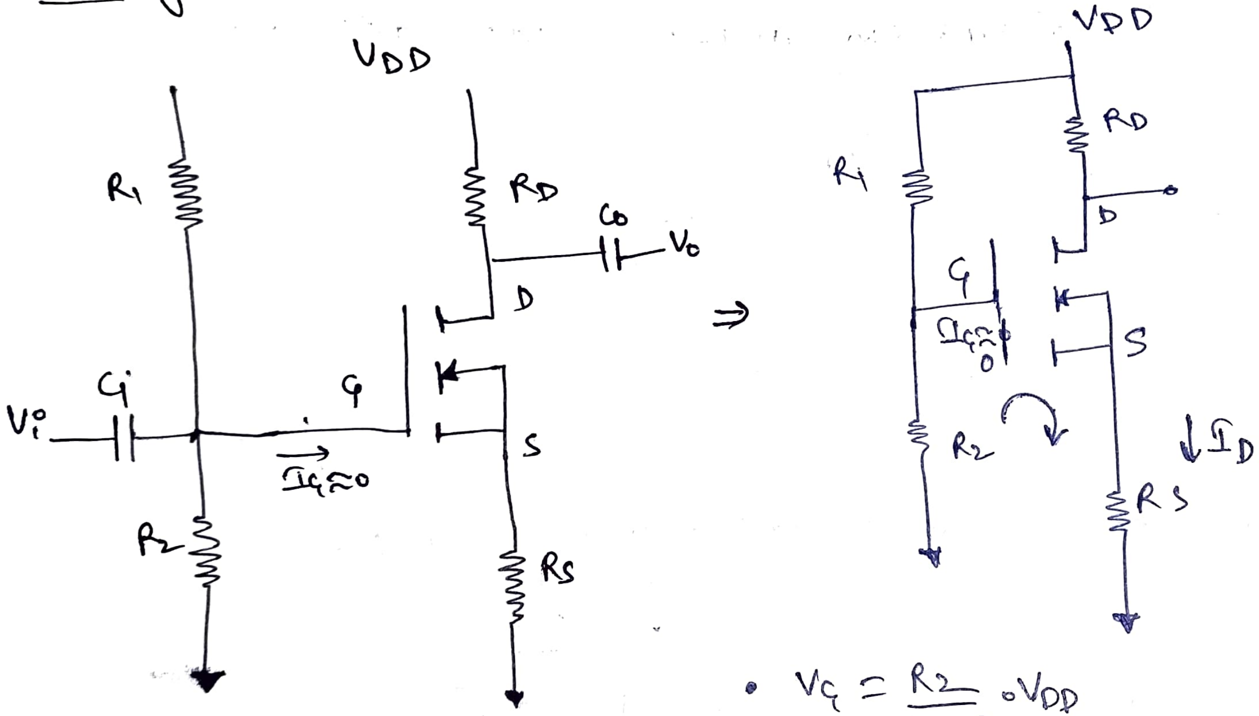
- $V_G = \frac{R_2}{R_1+R_2} \cdot V_{DD}$

- $V_{GS} = V_G - I_D R_S$
- $I_D = K(V_{GS} - V_T)^2$
- $I_D = \frac{1}{2} \mu_n C_{ox} \left[\frac{W}{L}\right] (V_{GS} - V_T)^2$

Transfer characteristics of Enhancement type MOSFET



Voltage Divider Biasing:-



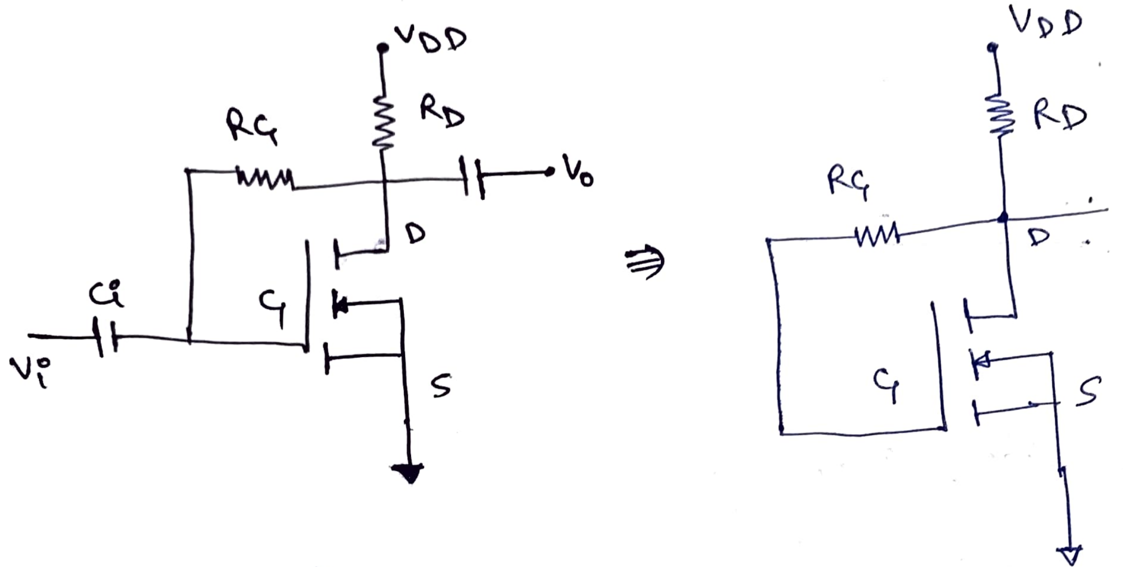
- $V_G = \frac{R_2}{R_1+R_2} \cdot V_{DD}$

- $V_{GS} = V_G - I_D R_S$
- $I_D = K(V_{GS} - V_T)^2$
- $I_D = \frac{1}{2} \mu_n C_{ox} \left[\frac{W}{L}\right] (V_{GS} - V_T)^2$

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

Drain feedback biasing :—



$$I_D = K(V_{GS} - V_T)^2$$

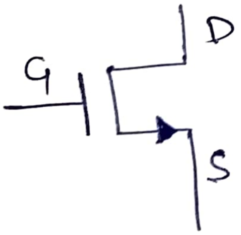
- $V_D = V_G$
- $V_{DS} = V_{GS} = V_{DD} - I_D R_D$

In sat. mode.

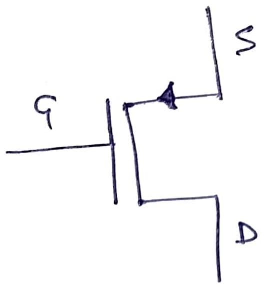
$$I_D = \frac{1}{2} \mu_n C_{ox} \left[\frac{W}{L}\right] (V_{GS} - V_T)^2$$

$$V_{GS} = V_{DD} - I_D R_D$$

Enhancement type MOSFET another symbols :—

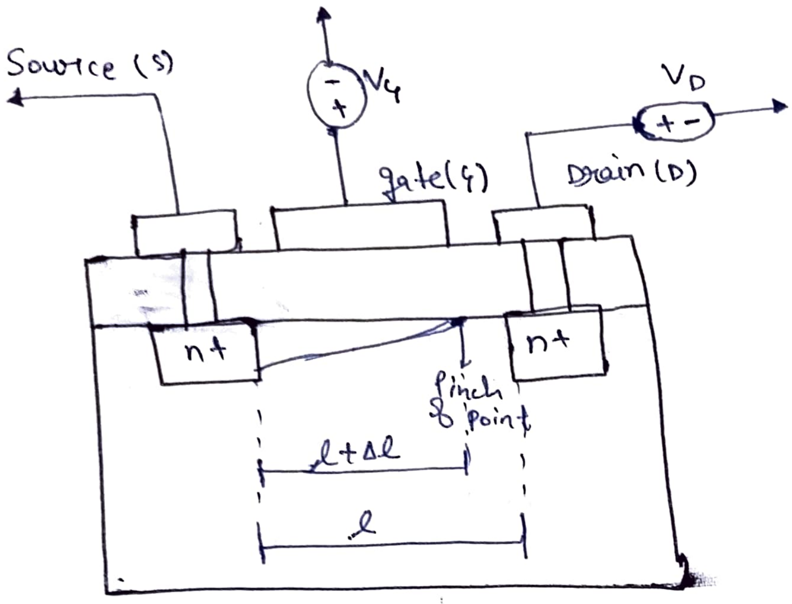


N - channel MOSFET



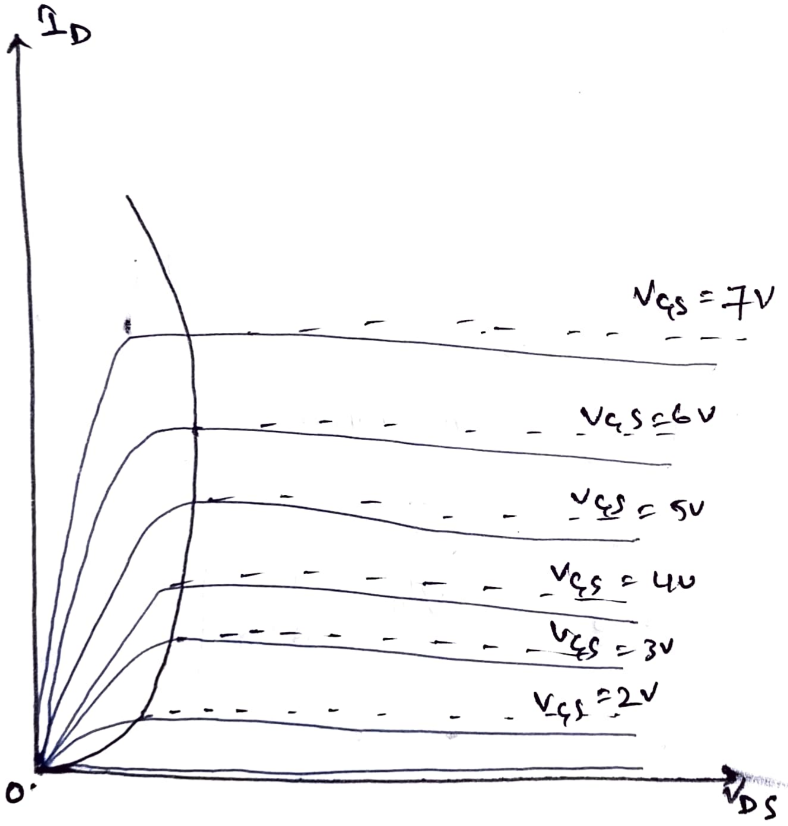
P - channel MOSFET

channel length Modulation :-



$V_{DS} \geq V_{GS} - V_T$

$$I_D = \frac{1}{2} \mu_n C_{ox} \left[\frac{W}{L}\right] (V_{GS} - V_T)^2$$



$$I_D = \frac{1}{2}\mu_n C_{ox}\left[\frac{W}{L}\right](V_{GS}-V_T)^2$$

$$= \frac{1}{2}\mu_n C_{ox}\left[\frac{W}{L - \Delta L}\right](V_{GS}-V_T)^2$$

$$= \frac{1}{2}\mu_n C_{ox}\left[\frac{W}{L}\right](V_{GS}-V_T)^2 \cdot \frac{1}{1-\frac{\Delta L}{L}}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_T)^2\left(1+\frac{\Delta L}{L}\right)$$

$l_{eff} = L - \Delta L$

$L - \Delta L = L\left[1 - \frac{\Delta L}{L}\right.$

$\frac{1}{1-\frac{\Delta L}{L}} = \left(1-\frac{\Delta L}{L}\right)^{-1}$

As $\Delta L << L$
then
$\left(1-\frac{\Delta L}{L}\right)^{-1} = \left(1+\frac{\Delta L}{L}\right)$

let, since $\Delta L \propto V_{DS}$

$\Rightarrow \Delta L = \lambda' V_{DS}$

$\frac{\Delta L}{L} = \frac{\lambda'}{L} V_{DS} = \lambda V_{DS}$

now,

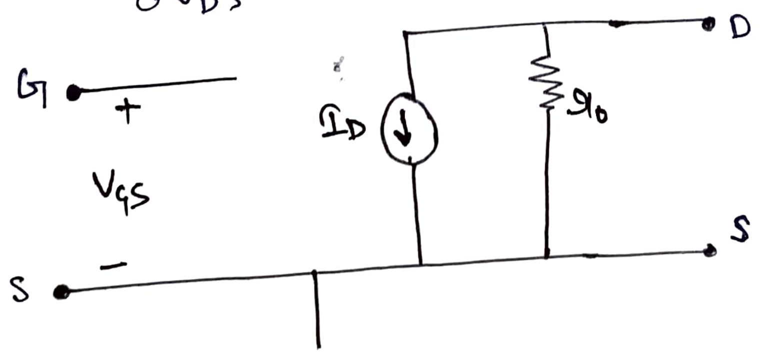
$$\boxed{I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS}-V_T)^2(1+\lambda V_{DS})}$$

$\Downarrow$

$I_D' = I_D(1+\lambda V_{DS})$ ← with channel length modulation

Now

$$\frac{1}{r_o} = \frac{\partial I_D'}{\partial V_{DS}} = \lambda I_D \Rightarrow \boxed{r_o = \frac{1}{\lambda I_D}}$$



3.

.if $V_{GS} < V_t$ → resistand = ∞

$$I_D = k_n' \left(\frac{W}{L}\right) \left(V_{OV} - \frac{1}{2} V_{DS}\right) V_{DS}$$

b $V_{GS} < V_t$ → resistand = ∞ 3

$$I_D = k_n' \left(\frac{W}{L}\right)\left(V_{OV} - \frac{1}{2}V_{DS}\right)V_{DS}$$

$V_{GS} > 0, \ V_{DS} = 0$

reshold voltage → 0.3 – 1 V (range) ← V_t

effective voltage or over derive Voltage :– $V_{OV} = V_{GS} - V_t$

Mag. of charge in the channel $|Q| = \underset{\substack{\uparrow \\ \text{oxide Capacitance}}}{C_{ox}}(WL) \cdot V_{OV}$

$$\Leftarrow C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \leftarrow \text{oxide thickness}$$

W → channel width

L → channel length

$\epsilon_{ox} = 3.9\,\epsilon_0 = 3.45 \times 10^{-11}$ f/m (for silicon oxide)

$C = C_{ox} W L$

Now applying small V_{DS} also:–

Source → grounded

$V_D \neq 0, \ V_G \neq 0$

flow of current → drain to source (i_D)

$$i_D = \frac{|Q|}{\text{unit channel length}} = C_{ox} W V_{OV}$$

electric field estabishes by V_{DS} across the channel length:–

$$|E| = \frac{V_{DS}}{L}$$

electron drift velocity $= \mu_n |E| = \mu_n \frac{V_{DS}}{L}$

$$i_D = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right) V_{ov}\right] V_{DS}$$

for small V_{DS}, channel behave like linear resistor which can be control by overdrive voltage in term of V_{GS}, so.

$$I_D = \left[(\mu_n C_{ox})\left(\frac{W}{L}\right)(V_{GS}-V_t)\right] V_{DS}$$

Conductance of channel

$$g_{DS} = (\mu_n C_{ox})\left(\frac{W}{L}\right) V_{ov}$$

or $$(\mu_n C_{ox})\left(\frac{W}{L}\right)(V_{GS}-V_t)$$

Process Conductance $k_n' = \mu_n C_{ox}$ unit (A/V^2)

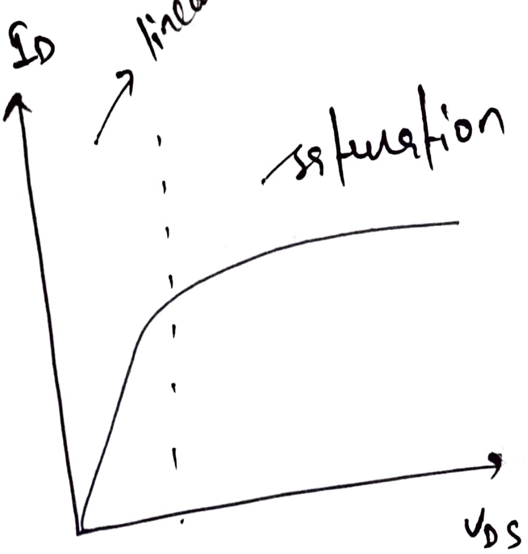
aspect ratio $\left(\frac{W}{L}\right)$

Transconductance $K_n = k_n'\left(\frac{W}{L}\right) = \mu_n C_{ox}\left(\frac{W}{L}\right) \rightarrow$ unit (A/V^2)

$$r_{DS} = \frac{1}{g_{DS}} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right) V_{ov}}$$

$$= \frac{1}{(\mu_n C_{ox})\left(\frac{W}{L}\right)(V_{GS}-V_t)}$$

ignal } channel Conductance.



= drain to source conductance (linear region).

$$_{ds} = \frac{\partial I_D}{\partial V_{DS}} , \quad r_{ds} = \frac{1}{g_{ds}}$$

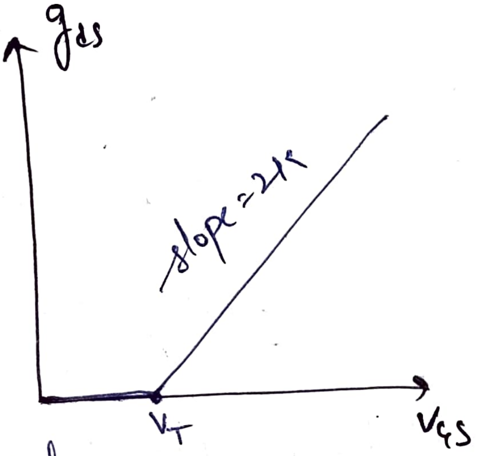
↑ channel resistance.

$$_D = 2K\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] ;$$ ← in linear region. $V_{DS} < V_{GS} - V_T$

for small V_{DS}, $\frac{V_{DS}^2}{2}$ ignored,

$$I_D = 2K\left[(V_{GS} - V_T) V_{DS}\right]$$

$$\boxed{g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = 2K(V_{GS} - V_T)}$$



before V_T MOSFET in cutoff Mode, there is no current channel conductance is zero.

Trans conductance :-

MOSFET acts as an amplifier in saturation Mode
↳ small signal Model

$$g_m = \frac{\partial I_D}{\partial V_{GS}} , \quad I_D = K(V_{GS} - V_T)^2 \longrightarrow$$

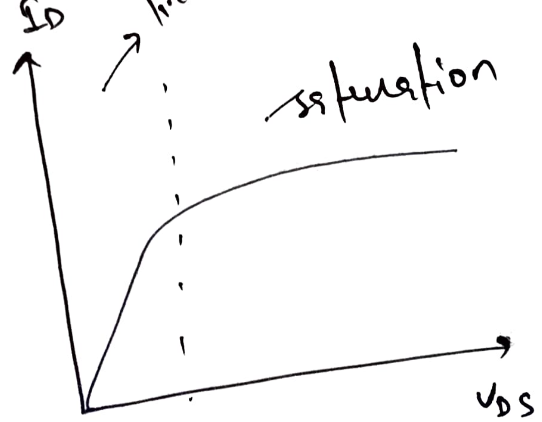
$$g_m = 2K[V_{GS} - V_T) , \quad K = \mu_n C_{ox} \frac{W}{2L}$$

all Signal } channel
odel

g_{ds} = drain to source conductance
(linear region).

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} , \quad \underset{\uparrow}{r_{ds}} = \frac{1}{g_{ds}}$$

channel resistance.



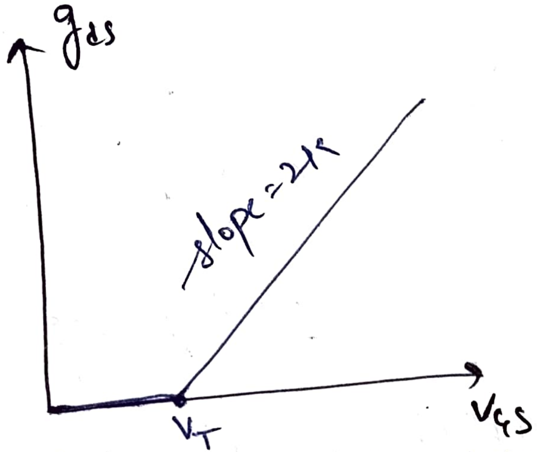
$$I_D = 2K\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] ; \quad V_{DS} < V_{GS} - V_T$$

← in linear region.

for small V_{DS}, $\frac{V_{DS}^2}{2}$ ignored,

$$I_D = 2K\left[(V_{GS} - V_T)\, V_{DS}\right]$$

$$\boxed{g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = 2K(V_{GS} - V_T)}$$



before V_T MOSFET in cutoff mode, there is no curre
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Transconductance :—

MOSFET acts as an amplifier in saturation mode
↳ small signal model

$$g_m = \frac{\partial I_D}{\partial V_{GS}} , \quad I_D = K(V_{GS} - V_T)^2 \longrightarrow$$

$$g_m = 2K\left[V_{GS} - V_T\right) , \quad K = \mu_n C_{ox} \frac{W}{2L}$$

$g_m = 2K\sqrt{\frac{I_D}{K}} = 2\sqrt{K I_D}$ from 'I_D' eqⁿ

O/p resistance :- $r_d = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\frac{\partial I_D}{\partial V_{DS}}}$ = high.

$$I_D = K(V_{GS}-V_T)^2 \underbrace{(1+\lambda V_{DS})}_{\text{from channel length modulation}}$$

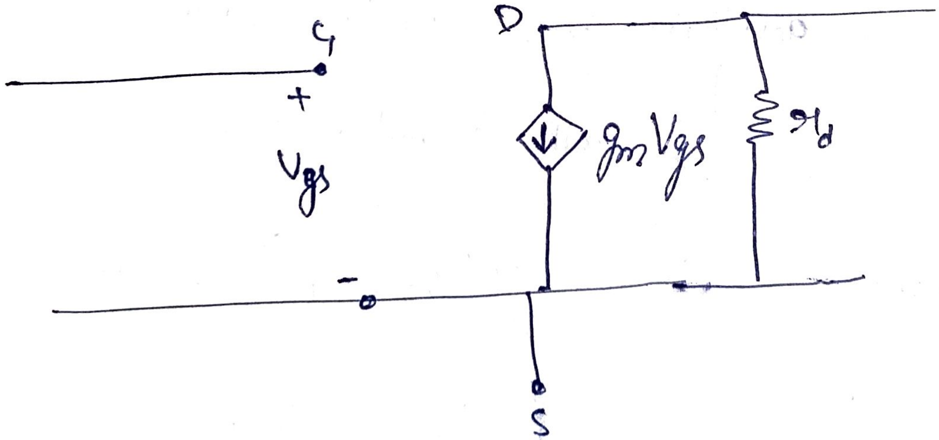
$$\frac{\partial I_D}{\partial V_{DS}} = K\lambda(V_{GS}-V_T)^2 \approx \lambda I_D$$

$$\boxed{r_d = \frac{1}{\lambda I_D}}$$

Small Signal Model

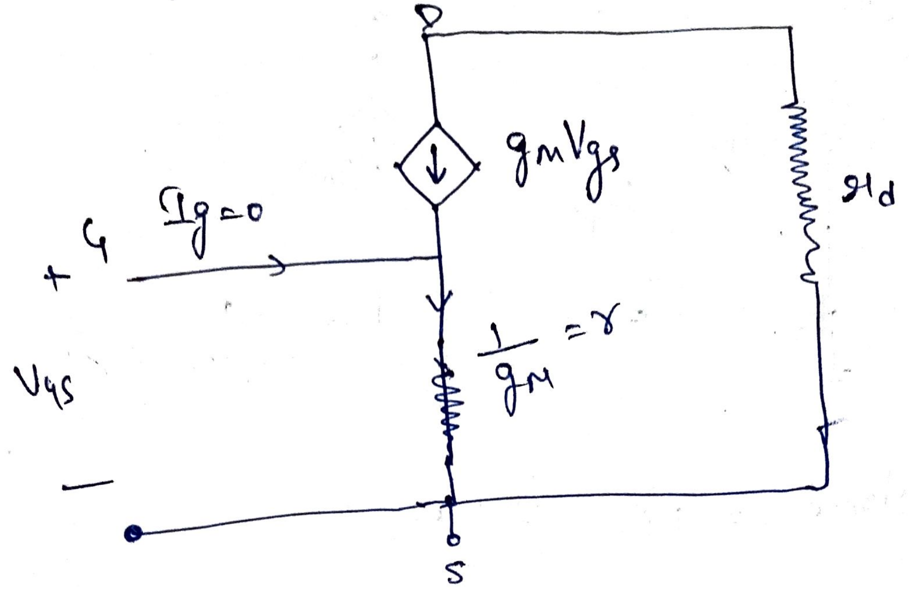
Hybrid - pi - Model :-

↳ gate terminal :- oxide layer is present
  ↳ I_g or $I_{in} = 0$; $Z_{in} \to \infty$ (open ckt)



T Model:-

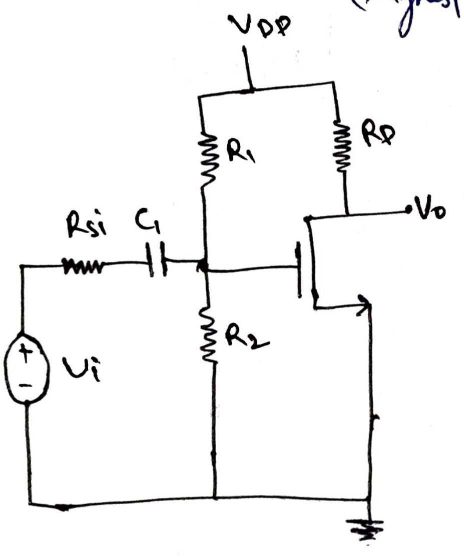
↳ small signal alternate model



Common Source amplifier:-

(highest voltage gain)

for dc analysis short ac, open ckt cap.



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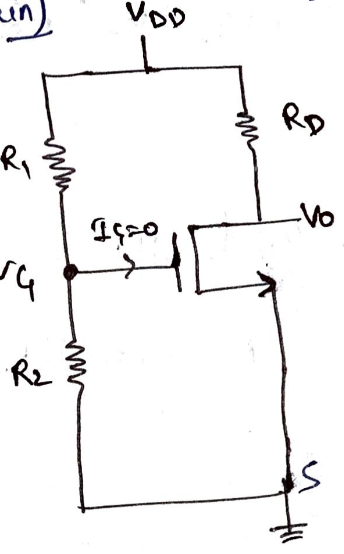


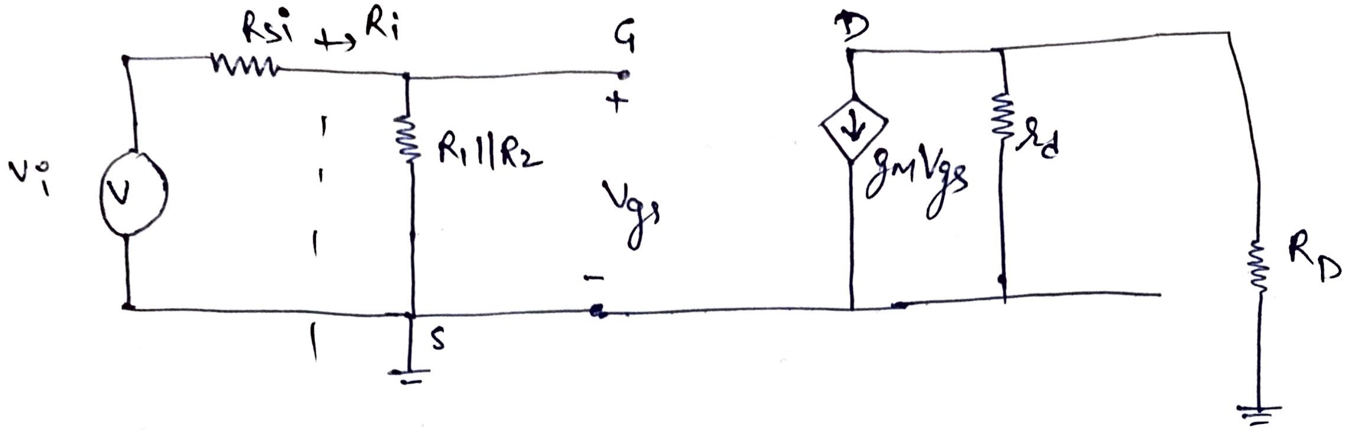
$V_G = \frac{V_{DD}R_2}{R_1+R_2}$, $\boxed{V_{GS} = V_G - \overset{\text{grounded}}{V_S} = V_G}$

$I_D = K(V_{GS}-V_t)^2$ (saturation)

$g_m = 2\sqrt{KI_D}$

for ac analysis:-

ground VDD, short ckt cap.



Input resistance = $R_i = R_1 || R_2$

output resistance :- $R_{out} = r_d || R_D \approx R_D$

$$V_o = -g_m V_{gs} (r_d || R_D) ; \quad V_{gs} = V_i \left(\frac{R_1 || R_2}{R_{si} + R_1 || R_2} \right)$$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m (r_o || R_D)(R_1 || R_2)}{R_{si} + (R_1 || R_2)}$$

if $R_{si} = 0$

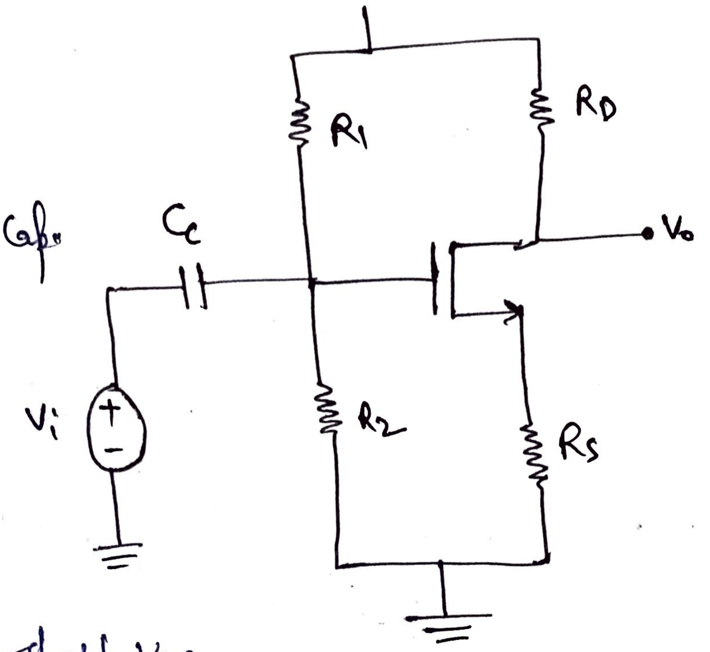
$$A_v = -g_m (r_o || R_D)$$

Common Source Amplifier

ypassed R_S → gain ↓

(-ve beedback)

tep 1 dc analysis :- oc Cap.

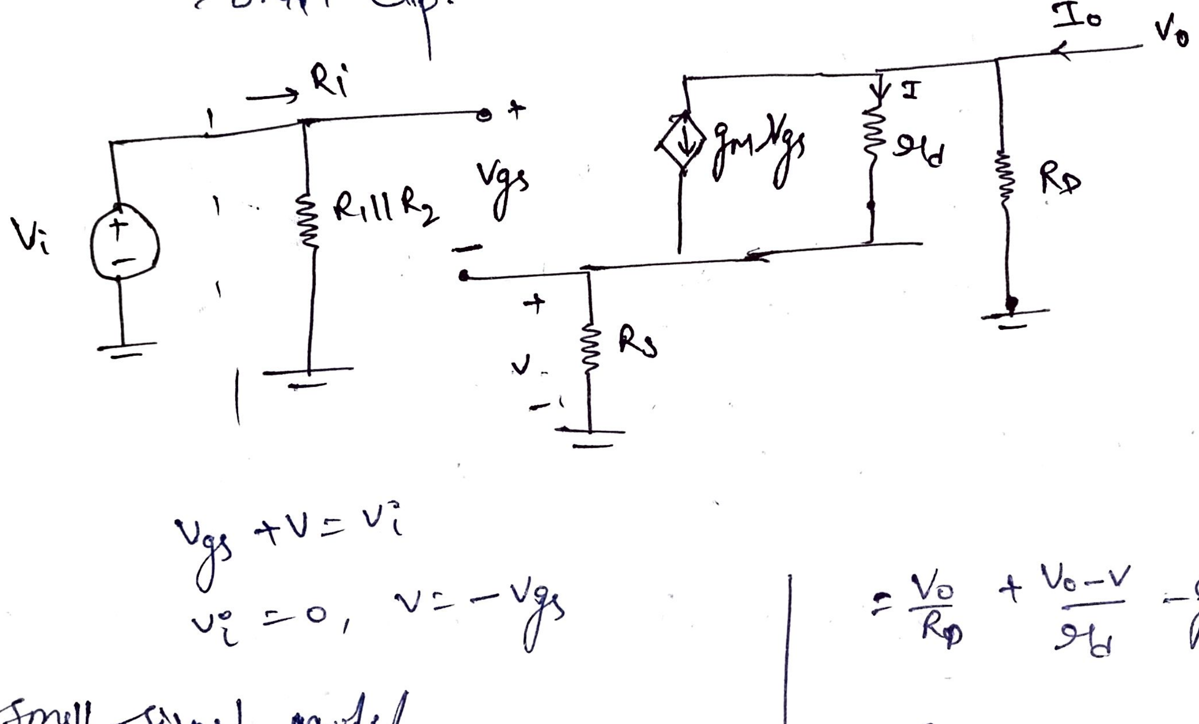


$I_D = ?$, $g_m = 2\sqrt{K I_D}$

$r_d = ?$

Step 2 :- ac analysis short VDD

short cap.



$V_{gs} + V = V_i$

$V_i = 0, \quad V = -V_{gs}$

Small signal model

Input resistance, $R_i = R_1 || R_2$

output resistance, $R_o = \frac{V_o}{I_o}\Big|_{V_i = 0}$

$I_o = \frac{V_o}{R_o} + \frac{V_o - V}{r_d} + g_m V_{gs}$

$= \frac{V_o}{R_D} + \frac{V_o - V}{r_d} - g_m V$

$V = (g_m V_{gs} + I) R_s$

$= -g_m V R_s + \frac{V_o - V}{r_d} R_s$

$= V\left[1 + g_m R_s + \frac{R_s}{r_d}\right] = \frac{V_o R_s}{r_d}$

$$V = \frac{\frac{V_o R_S}{r_d}}{1 + g_m R_s + \frac{R_S}{r_d}}$$

$$\Rightarrow I_o = \frac{V_o}{R_D} + \frac{V_o}{r_d} - V\left(g_m + \frac{1}{r_d}\right)$$

$$V_o\left[\frac{1}{R_D} + \frac{1}{r_d} - \frac{\left(g_m + \frac{1}{r_d}\right)\left(\frac{R_s}{r_d}\right)}{1 + g_m R_s + \frac{R_s}{r_d}}\right]$$

Ignore r_d, $\frac{1}{r_d} \rightarrow 0$

$R_{out} \approx R_D$.

Voltage gain (A_v), Ignore r_d

$V = g_m V_{gs} R_s$; $V_i = V_{gs} + V \Rightarrow V_{gs} = (1 + g_m R_s)$

$V_o = -g_m V_{gs} R_D$; $A_v = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_s}$

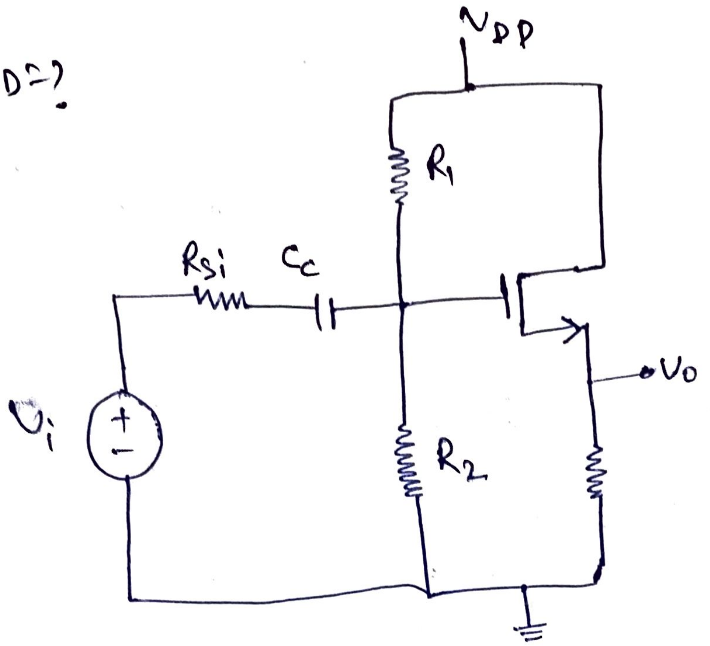
common Drain or source follower:—

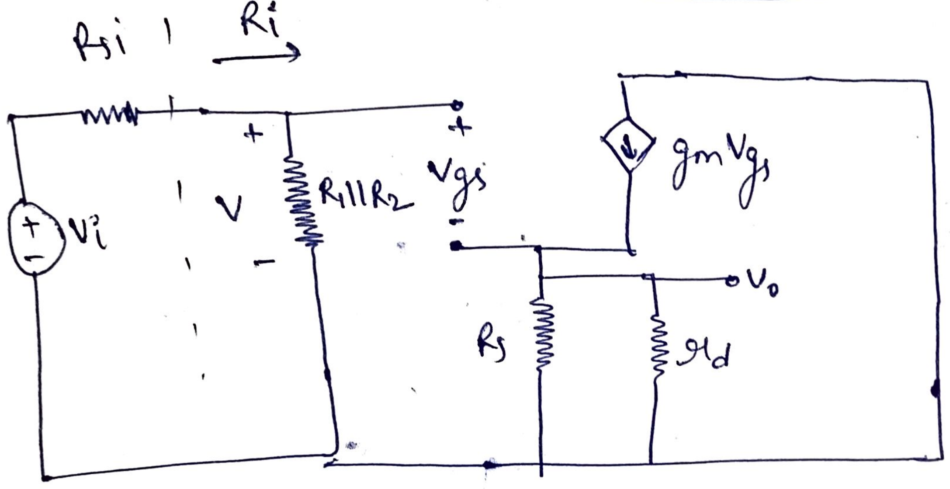
1:— perfor dc analysis, $I_D = ?$

$g_m = 2\sqrt{K I_D}$

p.2:— ground V_{DD},

short cap.





Input resistance: $R_i = R_1 \| R_2$

Small signal model:—

voltage gain $= \frac{V_o}{V_s}$.

$V_o = g_m V_{gs} (r_d \| R_s)$

$V = V_s \times \left(\frac{R_1 \| R_2)}{R_{si} + (R_1 \| R_2)} \right) = V_{gs} + V_o = V_{gs} \left(1 + g_m (r_d \| R_s) \right)$

$V_s = V_{gs} \left(1 + g_m (r_d \| R_s) \right) \times \frac{R_{si} + (R_1 \| R_2)}{(R_1 \| R_2)}$

$$A_{vs} = \frac{V_o}{V_s} = \underbrace{\frac{g_m(r_d \,||\, R_s)}{1+g_m(r_d \,||\, R_s)}}_{A_v} \left[\frac{R_1 \,||\, R_2}{R_{si} + R_1 \,||\, R_2}\right]$$

$A_{vs} = A_v$ if $R_{si} = 0$

$A_v < 1.$

output resistance:-

$$R_{out} = \left.\frac{V_o}{I_o}\right|_{v_{in}=0}$$

$$I_o - g_m V_o = \frac{V_o}{R_s} + \frac{V_o}{r_d}$$

$$I_o = \left(g_m + \frac{1}{R_s} + \frac{1}{r_d}\right) V_o$$

$$\frac{V_o}{I_o} = R_{out} = R_s \,||\, r_d \,||\, \frac{1}{g_m}$$

$$I_o + g_m V_{gs} = V_o/R_s + \frac{V_o}{r_d}$$

$$V = 0 = V_{gs} + V_o$$

$$\boxed{V_{gs} = -V_o}$$